Amendments to the Claims:

1. (currently amended) A method for accessing a memory to protect a memory section from being accessed or changed incorrectly when accessing the memory comprising:

~~(a)~~ generating a first logic address data;

~~(b)~~ selectively outputting the first logic address data or a second logic address data as a physical address data by using an address translator according to a control signal; ~~and~~

~~(c)~~ accessing the memory according to the physical address data; and

turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data when it is required to protect the memory section from being accessed;

wherein the second logic address data is a result obtained after operating on the first logic address data.

2. (currently amended) The method of claim 1 ~~wherein Step (b)~~ further ~~comprises~~ comprising operating on the first logic address data by using the address translator according to a setup value in order to generate the second logic address data.

3. (original) The method of claim 2 wherein the setup value is a value representing a characteristic of the memory section.

4. (original) The method of claim 2 wherein the setup value is stored in a register.

5. (currently amended) The method of claim 2 wherein the address translator further comprises an operating unit, and ~~Step (b)~~ the method further comprises operating on the first logic address data by using the operating unit according to the setup value to generate the second logic address data.

6. (currently amended) The method of claim 2 wherein the address translator further comprises a multiplexer, and the method ~~Step (b)~~ further comprises multiplexing the first logic address data and the second logic address data by using the multiplexer to selectively output the first logic address data or the second logic address data.

7. (currently amended) A microprocessor system for accessing a memory comprising:

a microprocessor for providing a first logic address data;

a memory comprising a first memory section and a second memory section; and

an address translator coupled between the microprocessor and the memory to selectively output the first logic address data or a second logic address data as a physical address data according to a control signal;

wherein the microprocessor is further for turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data when it is

required to protect the first memory section from being accessed; and

~~wherein~~ the second logic address data is a result obtained after operating on the first logic address data and the microprocessor accesses data of the first memory section or the second memory section according to the physical address data.

8. (currently amended) The microprocessor system ~~device~~ of claim 7 wherein the memory is a non-volatile memory.

9. (currently amended) The microprocessor system ~~device~~ of claim 7 wherein the address translator operates the first logic address data according to a setup value to generate the second logic address data.

10. (currently amended) The microprocessor system ~~device~~ of claim 9 wherein the setup value is a value representing a characteristic of the first memory section.

11. (currently amended) The microprocessor system ~~device~~ of claim 9 wherein the address translator further comprises an operating unit to operate on the first logic address data according to the setup value in order to generate the second logic address data.

12. (currently amended) The microprocessor system ~~device~~ of claim 9 wherein the address translator further comprises a register for storing the setup value.

13. (currently amended) The microprocessor system ~~device~~ of claim 7

wherein the address translator further comprises a multiplexer for multiplexing the first logic address data and the second logic address data in order to selectively output the first logic address data or the second logic address data.

14. (new) The method of claim 5, wherein the operating unit of the address translator is an adder.

15. (new) The method of claim 1, wherein the memory section comprises boot code for a microprocessor, the microprocessor for generating the first logic address data.

16. (new) The method of claim 15, further comprising:

turning off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when power is turned on or restored to the microprocessor to thereby allow access to the boot code; and

when the microprocessor has successfully booted the system according to the boot code, turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data to thereby protect the boot code from being accessed.

17. (new) The method of claim 15, further comprising turning off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when it is required to erase or update the boot code to thereby allow access to the

boot code in the memory section by the microprocessor.

18. (new) The microprocessor system of claim 11, wherein the operating unit of the address translator is an adder.

19. (new) The microprocessor system of claim 7, wherein the first memory section comprises boot code for the microprocessor.

20. (new) The microprocessor system of claim 19, wherein the microprocessor is further for turning off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when power is turned on or restored to the microprocessor to thereby allow access to the boot code; and when the microprocessor has successfully booted the system according to the boot code, for turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data to thereby protect the boot code from being accessed.

21. (new) The microprocessor system of claim 19, wherein the microprocessor is further for turning off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when it is required to erase or update the boot code to thereby allow access to the boot code in the first memory section by the microprocessor.